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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/671,065 35525	09/28/2000 7590	Michael Anthony Perez 02/23/2004	AUS9-2000-0452-US1	7603
			EXAMINER	VO, TIM T
DUKE W. YEE CARSTENS, YEE & CAHOON, L.L.P. P.O. BOX 802334 DALLAS, TX 75380			ART UNIT	PAPER NUMBER
			2112	9
			DATE MAILED: 02/23/2004	

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)
	09/671,065	PEREZ, MICHAEL ANTHONY
Examiner	Art Unit	
Tim T. Vo	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### **Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

1)  Responsive to communication(s) filed on 11 December 2003.

2a)  This action is **FINAL**.                            2b)  This action is non-final.

3)  Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## **Disposition of Claims**

4)  Claim(s) 1-5 and 7-28 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

5)  Claim(s) 1-5, 7, 15-19 and 22-26 is/are allowed.

6)  Claim(s) 8-14, 20, 21, 27 and 28 is/are rejected.

7)  Claim(s) \_\_\_\_\_ is/are objected to.

8)  Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

9)  The specification is objected to by the Examiner.

10)  The drawing(s) filed on \_\_\_\_\_ is/are: a)  accepted or b)  objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)  The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)  Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a)  All    b)  Some \* c)  None of:  
1.  Certified copies of the priority documents have been received.  
2.  Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3.  Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1)  Notice of References Cited (PTO-892)  
2)  Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3)  Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date

4)  Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_ .

5)  Notice of Informal Patent Application (PTO-152)

6)  Other: \_\_\_\_\_

***Responses to Arguments***

1. Applicant's arguments with respect to claims 1-5 and 7-28 have been considered but are moot in view of the new ground(s) of rejection.

**Part III DETAILED ACTION**

***Notice to Applicant(s)***

This application has been examined. Claims 1-5 and 7-28 are pending.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 8-14, 20-21 and 27-28 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Anderson et al. patent number 6,338,119 referred hereinafter "Anderson" in view of Linam et al. patent number 6,658,559 referred hereinafter "Linam".

As for claims 8, 20 and 27, Anderson teaches a method of providing data to an I/O adapter from a bus bridge (see figure 1, bus bridge 108, I/O devices 118, 120 and column 5 lines 8-11, wherein the bus bridge 108 are transferring data to the I/O devices 118, 120 via a conventional adapter), the method comprising:

receiving a request for data from the I/O adapter (see figure 1, bridge 108 and column 7 lines 8-10 and column 7 lines 45-49, wherein figure 1 discloses I/O devices 118, 120 which are communicating with symmetric multi-processors (SMP) 102 via bridge 108 and conventional adapter and vice versa for the SMP to communicate with the I/O devices 118, 120. Further, bridge 108 maintains cache 109 coherency as cited in column 4 lines 63-67);

responsive to a determination that the requested data is contained within a cached memory (see figure 1, cache 109), providing the requested data using the data in the cached memory (see figure 1, bridge 108, cache 109, figure 4 step 406 and 7 lines 6-10, wherein the bridge 108 determined whether cache 109 is valid or invalid).

Anderson does not expressly teach bridge 108 is a pci-pci bridge as claimed. However, a pci-pci bridge is well known and expected in the art for supporting plug and play during operation. Linam teaches pci-pci bridge allows hot plugging for system addition, removal, and replacement during operation (see column 3 lines 40-58 of Linam). It would have been obvious to utilize the pci-pci bridge of Linam to provide hot plugging to support Anderson's system for expansion, maintenance and repair to minimize disruption of the system operation.

As for claims 9, 21 and 28, Anderson teaches responsive to a determination that the requested data is not contained within the cached memory (see figure 1, I/O 118, 120, memory 110 and column 5 lines 1-7, wherein the I/O devices 118, 120 are transferring data to and from system memory 110).

storing the data received from the system memory in the cached memory (see figure 1, system memory containing 130-136 buffers and column 5 lines 22-33, wherein the data are transferred from buffers 130-136 of system memory to cache); and

providing at least a portion of the data received from the system memory to the requesting I/O adapter (see figure 1, I/O 118, 120, system memory 110 and column 5 lines 1-7, wherein I/O devices 118, 120 are transferring data to and from system memory 110).

As for claim 10, Anderson teaches a bridge (see figure 1, I/O devices 118, 120, conventional adapter and column 5 lines 1-11, wherein I/O devices 118, 120 are connected to conventional adapter i.e. bridge), comprising:

an interface for sending and receiving data from a bridge (see figure 1, bridge 108 and column 5 lines 1-12, wherein data communication are transferring between system memory 110 and I/O devices 118, 120 via bridge 108 and conventional adapter);

an interface for sending and receiving data from an input/output adapter (see figure 1, bridge 108 and column 5 lines 1-12, wherein data communication are transferring between system memory 110 and I/O devices 118, 120 via bridge 108 and conventional adapter);

buffers for storing data (see cache 109, system memory 110);

an interface for receiving signals from the bridge indicating whether data in the buffers are stale (see figure 4, step 406 and column 7 lines 8-22, wherein the bridge determines whether cache 109 is invalid i.e. stale); and

logic for clearing stale data from the buffers and retrieving fresh data from the bridge(see column 4 lines 63-67 and column 5 lines 27-33, wherein one of the embodiment, Anderson teaches the bridge maintains cache coherency across L1/L2 caches and cache 109 by clearing buffer memory in cache 109 to make room for new data).

Anderson does not expressly teach bridge 108 is a pci-pci bridge as claimed. However, a pci-pci bridge is well known an expected in the art for supporting plug and play during operation. Linam teaches pci-pci bridge allows hot plugging for system addition, removal, and replacement during operation (see column 3 lines 40-58 of Linam). It would have been obvious to utilize the pci-pci bridge of Linam to providing hot plugging to support Anderson's system for expansion, maintenance and repair to minimize disruption of the system operation.

As for claims 11-14, Anderson teaches an interface for receiving signals from the bridge selecting one of a plurality of modes for handling stale data in the peripheral component interconnect to peripheral component interconnect bridge (see figure 4, step 406 and column 7 lines 8-22, wherein the bridge determines whether cache 109 is invalid i.e. stale and see column 4 lines 63-67 and column 5 lines 27-33, wherein one of the embodiment, Anderson teaches the bridge maintains cache coherency across L1/L2 caches and cache 109 by clearing buffer memory in cache 109 to make room for new data).

### ***Examiner's Statement of Reasons for Allowance***

1. Claims 1-5, 7, 15-19 and 22-26 are allowable over the prior of records.

2. The following is an Examiner's statement of reasons for the indication of allowable subject matter: Claims 1, 15 and 22 are allowable over the prior art of record because the Examiner found neither prior art cited in its entirety, nor based on the prior art, found any motivation to combine any of the said prior arts. Prior art fails to teach a host bridge determining whether the cache located in the PCI to PCI bridge is fresh or stale and if the cache is stale, clearing at least the portion of the cached memory containing the stale data.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tim T. Vo whose telephone number is 703-308-5862. The examiner can normally be reached on 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Tim T. Vo  
Primary Examiner  
Art Unit 2112

February 19, 2004